Amendments to the Specification:

Please replace paragraph [0026] with the following amended paragraph:

[0026] In embodiments according to the present invention, the depth of the recessed region is a predetermined depth. In the embodiment illustrated in FIG. 3B, the depth ~~332~~ 322 of the recessed regions is 0.5 mm. Alternatively, the depth ranges from about 0.1 mm to about 1 mm in other embodiments. Of course, the depth of the recessed region will depend on the particular applications. Additionally, in embodiments according to the present invention, the area of the individual recessed regions will be a predetermined size. In the embodiment illustrated in FIG. 3B, the area of the individual recessed regions is about 14 mm x 18 mm. Depending on the specific applications, this area may vary in size.

Please replace paragraph [0038] with the following amended paragraph:

[0038] In an embodiment according to the present invention, hermetically sealed die-level packages are formed by coupling the transparent member to the substrate. FIG. 3C is a simplified diagram of the transparent member and the substrate at the time of hermetic sealing. The transparent member is aligned in a manner to position the standoff regions 340 and 342 above the street regions 344 and 346. The individual chips 350 are located below and in communication with an associated recessed region 352 and hermetically sealed by the transparent cover 354 at contact points 356 located at the base of the standoff regions 342. Through holes ~~354~~ 348 provide access to bond pads 358 located on the CMOS wafer.